

ABSTRACT

A fast data access circuit that has both a standard clock mode and a fast data access mode. The mode is selectable through a mode/configuration register. A configuration word loaded into the register has bits to indicate the desired mode and the input clock frequency. In the fast data access mode, a clock delay circuit uses the clock frequency setting bits to select a delay to be added to the input clock. The higher the clock frequency, the less the added delay. The delayed clock generates FIFO control signals to control a data FIFO register. During the fast data access mode, the data is output from the data FIFO register at a faster rate than in the standard clock mode.